

# WiP: Towards a Secure SECP256K1 for Crypto Wallets: Hardware Architecture and Implementation

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## Outline

- Background
- Motivation
- Objectives
- Contributions
- Results
- Conclusion













Applications: Supply chain management, Internet of things, Cryptocurrency (Crypto)



























#### Bitcoin and Ethereum wallets







#### Bitcoin and Ethereum wallets



Computes a public key given a private key





#### Bitcoin and Ethereum wallets



Various attacks targeted Elliptic curve cryptography (ECC) algorithm.





SECP256K1





#### Key vulnerability in Montgomery ladder ECPM

Algorithm 1 Montgomery Ladder **Input:**  $P \in (x, y, z), m = (m_{t-1}, \ldots, m_0)$  with  $m_{t-1} = 1$ Output: R = mPInitialisation: 1:  $R_0 \leftarrow P$ 2:  $R_1 \leftarrow 2P$ Loop Process: Power consumption pattern and 3: for i = t - 2 to 0 do execution time discrepancy  $\begin{array}{c} \text{if } m_i = 1 \text{ then} \\ R_0 \leftarrow R_0 + R_1 \\ R_1 \leftarrow 2R_1 \end{array} \quad \mathsf{Private key bit = 1} \end{array}$ 4: 5: 6: 7. else  $R_1 \leftarrow R_0 + R_1$  Private key bit = 0 8: 9: 10:end if 11: end for 12: return  $R_0$ 

#### Objectives

- To secure SECP256K1 against side-channel analysis (SCA) attack.
  - Complete addition equation
  - Temporary registers
  - Parallel operations
- To minimize resources utilized by SECP256K1.
  - Efficiently reusing modules





#### Use equations to perform ECPA

Algorithm 2 Equations for complete, projective point addition for SECP256K1

**Input:**  $P = (X_1, Y_1, Z_1), Q = (X_2, Y_2, Z_2)$  on  $E : Y^2 Z = X^3 + bZ^3$  and  $b_3 = 3 \cdot b$ . **Output:**  $(X_3, Y_3, Z_3) = P + Q$ ;

| 1:  | $t_0 \leftarrow X_1 \cdot X_2$ | 12: $X_3 \leftarrow t_1 + t_2$     | 23: | $t_1 \leftarrow t_1 - t_2$     |
|-----|--------------------------------|------------------------------------|-----|--------------------------------|
| 2:  | $t_1 \leftarrow Y_1 \cdot Y_2$ | 13: $t_4 \leftarrow t_4 - X_3$     | 24: | $Y_3 \leftarrow b_3 \cdot Y_3$ |
| 3:  | $t_2 \leftarrow Z_1 \cdot Z_2$ | 14: $X_3 \leftarrow X_1 + Z_1$     | 25: | $X_3 \leftarrow t_4 \cdot Y_3$ |
| 4:  | $t_3 \leftarrow X_1 + Y_1$     | 15: $Y_3 \leftarrow X_2 + Z_2$     | 26: | $t_2 \leftarrow t_3 \cdot t_1$ |
| 5:  | $t_4 \leftarrow X_2 + Y_2$     | 16: $X_3 \leftarrow X_3 \cdot Y_3$ | 27: | $X_3 \leftarrow t_2 - X_3$     |
| 6:  | $t_3 \leftarrow t_3 \cdot t_4$ | 17: $Y_3 \leftarrow t_0 + t_2$     | 28: | $Y_3 \leftarrow Y_3 \cdot t_0$ |
| 7:  | $t_4 \leftarrow t_0 + t_1$     | 18: $Y_3 \leftarrow X_3 - Y_3$     | 29: | $t_1 \leftarrow t_1 \cdot Z_3$ |
| 8:  | $t_3 \leftarrow t_3 - t_4$     | 19: $X_3 \leftarrow t_0 + t_0$     | 30: | $Y_3 \leftarrow t_1 + Y_3$     |
| 9:  | $t_4 \leftarrow Y_1 + Z_1$     | 20: $t_0 \leftarrow X_3 + t_0$     | 31: | $t_0 \leftarrow t_0 \cdot t_3$ |
| 10: | $X_3 \leftarrow Y_2 + Z_2$     | 21: $t_2 \leftarrow b_3 \cdot t_2$ | 32: | $Z_3 \leftarrow Z_3 \cdot t_4$ |
| 11: | $t_4 \leftarrow t_4 \cdot X_3$ | 22: $Z_3 \leftarrow t_1 + t_2$     | 33: | $Z_3 \leftarrow Z_3 + t_0$     |
|     |                                |                                    |     |                                |

#### Avoid the branching caused by SECP256K1 EC addition operation





#### Use temporary registers in ECPM

Algorithm 3 Montgomery Ladder Algorithm with Temporary Registers **Input:**  $P \in (x, y, z), m = (m_{t-1}, \dots, m_0)$  with  $m_{t-1} = 1$ Output: R = mPInitialisation: 1:  $R_0 \leftarrow P$ 2:  $\mathbf{R}_1 \leftarrow 2\mathbf{P}$ Loop Process: 3: for i = t - 2 to 0 do if  $m_i = 1$  then  $\begin{array}{c|c} \mathbf{R}_{0} \leftarrow \mathbf{R}_{0} + \mathbf{R}_{1} \\ \mathbf{R}_{1} \leftarrow 2\mathbf{R}_{1} \end{array} \quad \text{Private key bit = 1}$ 5: 6:  $R_t \leftarrow 2R_0$ 7:  $egin{aligned} \mathbf{else} & & \ & \mathbf{R_1} \leftarrow \mathbf{R_0} + \mathbf{R_1} \ & & \ & \mathbf{R_0} \leftarrow 2\mathbf{R_0} \end{aligned}$ 8: Private key bit = 0 9. 10:  $\mathbf{R}_{t} \leftarrow 2\mathbf{R}_{1}$ 11: end if 12: 13: end for 14: return Ro

#### Both branches perform addition and doubling of the same registers





#### Use parallel operation in hardware implementation



- **1** ECPM done in projective coordinates.
- Ø Binary inversion done at the end.
- S ECPA is done with two modules in parallel.
- O Registers reused to achieve minimum area.



#### SECP256K1 implementation results

| Work                  | Platform |      | Area Frequency Latency |             | ency      | Throughput <sup>a</sup> |      |       |        |
|-----------------------|----------|------|------------------------|-------------|-----------|-------------------------|------|-------|--------|
|                       |          | kLUT | DSP                    | RAM (kbits) | Registers | (MHz)                   | (ms) | (kCC) | (kbps) |
| This work             | Zynq-US  | 21   | 0                      | 0           | 13 881    | 250                     | 7.58 | 1895  | 34     |
| This work             | Artix-7  | 24   | 0                      | 0           | 13 385    | 90                      | 21   | 1895  | 12     |
| Mehrabi et al.[1]     | Virtex-7 | 47   | 560                    | 0           | 29742     | 125                     | 0.25 | N/A   | N/A    |
| Asif et al.[2]        | Virtex-7 | 19   | 1036                   | 828         | N/A       | 87                      | 0.73 | 63    | 351    |
| Islam et al.[3]       | Virtex-7 | 36   | N/A                    | N/A         | N/A       | 178                     | 1.48 | 2630  | 173    |
| Romel et al.[4]       | Virtex-7 | 52   | 0                      | N/A         | 15263     | 122                     | 0.54 | 66    | 476    |
| Arunachalam et al.[5] | Virtex-5 | 33   | N/A                    | N/A         | N/A       | 192                     | 1.21 | 232   | 212    |
| Roy et al.[6]         | Virtex-5 | 40   | 0                      | N/A         | N/A       | 43                      | 0.60 | 26    | 1 667  |
| Asif et al.[7]        | Virtex-7 | 97   | 2799                   | 7 452       | N/A       | 73                      | 2.96 | 216   | 1816   |

<sup>a</sup> Throughput is estimated by authors as (Frequency  $\div$  CC)  $\times$  256.



#### Power side channel analysis



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#### Conclusion

- Temporary registers and parallel operation used to mitigate SCA.
- MSE is small, suggesting protection against differential power analysis.
- Proposed architecture uses few resources.
- Future: Hardware architecture for a crypto wallet.





# Thank you!





## Refferences

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